IN THE CLAIMS:

The text of all pending claims (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please ADD new claims 34-36 in accordance with the following:

1. (PREVIOUSLY PRESENTED) A testing apparatus for an integrated circuit comprising:

a pattern generator built in said integrated circuit to generate pseudo random patterns as test patterns;

a plurality of shift registers configured with sequential circuit elements inside said integrated circuit;

an automatic test pattern generating unit to generate ATPG patterns; and

a pattern modifier to modify a portion, to which a predetermined value is required to be set in order to detect a fault, in said pseudo random patterns generated by said pattern generator, on a basis of said ATPG patterns, by interpolating said pseudo random patterns with said ATPG patterns, and to input said modified pseudo random patterns to said shift registers.

2. (PREVIOUSLY PRESENTED) A testing apparatus for an integrated circuit comprising:

a plurality of shift registers, to which test patterns are inputted, configured with sequential circuit elements inside said integrated circuit;

a mask to convert an indeterminate value in outputs from said shift registers into a state value of "0" or "1" to mask said indeterminate value; and

an output verifier to verify output results in which said indeterminate value is masked by said mask, said output results not containing said indeterminate value.

3. (PREVIOUSLY PRESENTED) A testing apparatus for an integrated circuit comprising:

a pattern generator built in said integrated circuit to generate pseudo random patterns as test patterns;

a plurality of shift registers configured with sequential circuit elements inside said

integrated circuit;

an automatic test pattern generating unit to generate ATPG patterns;

a pattern modifier to modify a portion, to which a predetermined value is required to be set in order to detect a fault, in said pseudo random patterns generated by said pattern generator, on a basis of said ATPG patterns, by interpolating said pseudo random patterns with said ATPG patterns, and to input said modified pseudo random patterns to said shift registers;

a mask to convert an indeterminate value in outputs from said shift registers into a state value of "0" or "1" to mask said indeterminate value; and

an output verifier to verify output results in which said indeterminate value is masked by said mask, said output results not containing said indeterminate value.

4. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 2, wherein said output verifier includes a compressing means for compressing said masked output results.

5. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 3, wherein said output verifier includes a compressing means for compressing said masked output results.

6. (PREVIOUSLY PRESENTED) A testing method for an integrated circuit comprising:

generating pseudo random patterns as test patterns by a pattern generator built in said integrated circuit;

generating ATPG patterns;

modifying a portion, to which a predetermined value is required to be set in order to detect a fault, in said generated pseudo random patterns on a basis of said ATPG patterns, by interpolating said pseudo random patterns with said ATPG patterns; and

inputting said modified pseudo random patterns to a plurality of shift registers configured with sequential circuit elements inside said integrated circuit.

7-8. (CANCELLED)

9. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 1, wherein said pattern modifier selects a suitable combination of one pseudo random pattern and

one ATPG pattern from said pseudo random patterns generated by said pattern generator and said ATPG patterns, and modifies said selected pseudo random pattern on the basis of said selected ATPG pattern.

10. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 3, wherein said pattern modifier selects a suitable combination of one pseudo random pattern and one ATPG pattern from said pseudo random patterns generated by said pattern generator and said ATPG patterns, and modifies said selected pseudo random pattern on the basis of said selected ATPG pattern.

11. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 1, wherein said automatic test pattern generating unit refers to each of said pseudo random patterns generated by said pattern generator, selects a suitable target fault according to each of said pseudo random patterns, and generates an ATPG pattern, with which said target fault can be detected, as a reference for modifying each of said pseudo random patterns.

12. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 3, wherein said automatic test pattern generating unit refers to each of said pseudo random patterns generated by said pattern generator, selects a suitable target fault according to each of said pseudo random patterns, and generates an ATPG pattern, with which said target fault can be detected, as a reference for modifying each of said pseudo random patterns.

13. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 1 further comprising:

a characteristic information determining unit to compare said pseudo random patterns generated by said pattern generator with said ATPG patterns to determine characteristic information on said pattern generator with which said pattern generator can generate pseudo random patterns analogous to said ATPG patterns;

wherein said pattern generator generates said pseudo random patterns on the basis of said characteristic information determined by said characteristic information determining unit.

14. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 3 further comprising:

a characteristic information determining unit to compare said pseudo random patterns

generated by said pattern generator with said ATPG patterns to determine characteristic information on said pattern generator with which said pattern generator can generate pseudo random patterns analogous to said ATPG patterns;

wherein said pattern generator generates said pseudo random patterns on the basis of said characteristic information determined by said characteristic information determining unit.

15. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 13, wherein said characteristic information is a seed value to be set to said pattern generator.

16. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 14, wherein said characteristic information is a seed value to be set to said pattern generator.

17. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 13, wherein said pattern generator is configured as a linear feedback shift register, and said characteristic information is a feedback position in said linear feedback shift register.

18. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 14, wherein said pattern generator is configured as a linear feedback shift register, and said characteristic information is a feedback position in said linear feedback shift register.

19. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 1 further comprising an execution limitation condition setting unit for setting, when said automatic test pattern generating unit executes a compressing process on said ATPG pattern, an execution limitation condition for limiting the execution of said compressing process;

wherein said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when said execution limitation condition set by said execution limitation condition setting unit is satisfied.

20. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 3 further comprising an execution limitation condition setting unit for setting, when said automatic test pattern generating unit executes a compressing process on said ATPG pattern, an execution limitation condition for limiting the execution of said compressing process;

wherein said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when said execution limitation condition set by said execution limitation

condition setting unit is satisfied.

21. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 19, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper limit value of the number of faults to be detected with one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when the number of detection target faults, that are compressed in said ATPG pattern by said compressing process, reaches said upper limit value.

22. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 20, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper limit value of the number of faults to be detected with one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when the number of detection target faults, that are compressed in said ATPG pattern by said compressing process, reaches said upper limit value.

23. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 21, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses.

24. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 22, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses.

25. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 19, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper value of a quantity of pattern modification by said pattern modifier in the case where said pattern modifier modifies one of said pseudo random patterns on the basis of one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when a quantity of pattern modification, performed by said pattern modifier in the case where said pattern modifier modifies said pseudo random pattern on the basis of one ATPG pattern in which detection target faults are compressed by said compressing process, reaches said upper limit value.

26. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 20, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper value of a quantity of pattern modification by said pattern modifier in the case where said pattern modifier modifies one of said pseudo random patterns on the basis of one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when a quantity of pattern modification, performed by said pattern modifier in the case where said pattern modifier modifies said pseudo random pattern on the basis of one ATPG pattern in which detection target faults are compressed by said compressing process, reaches said upper limit value.

27. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 25, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses.

28. (PREVIOUSLY PRESENTED) The testing apparatus according to claim 26, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses.

29. (PREVIOUSLY PRESENTED) An integrated circuit including sequential circuit elements having:

a plurality of shift registers configured with said sequential circuit elements;

a pattern generator to generate pseudo random patterns as test patterns;

an automatic test pattern generating unit to generate ATPG patterns; and

a pattern modifier to modify a portion, to which a predetermined value is required to be set in order to detect a fault, in said pseudo random patterns generated by said pattern generator, on a basis of said ATPG patterns given from said automatic test pattern generating unit, by interpolating said pseudo random patterns with said ATPG patterns, and to input said modified pseudo random patterns to said shift registers.

30. (PREVIOUSLY PRESENTED) An integrated circuit including sequential circuit elements having:

a plurality of shift registers, to which test patterns are inputted, configured with said sequential circuit elements;

a mask to convert an indeterminate value in outputs from said shift registers into a state

value of "0" or "1" to mask said indeterminate value; and

an output verifier to verify output results in which said indeterminate value is masked by said mask, said output results not containing said indeterminate value.

31. (PREVIOUSLY PRESENTED) An integrated circuit including sequential circuit elements having:

a plurality of shift registers configured with said sequential circuit elements;

a pattern generator to generate pseudo random patterns as test patterns;

an automatic test pattern generating unit to generate ATPG patterns;

a pattern modifier to modify a portion, to which a predetermined value is required to be set in order to detect a fault, in said pseudo random pattern generated by said pattern generator, on a basis of said ATPG patterns given from said automatic test pattern generating unit, by interpolating said pseudo random pattern with said ATPG patterns, and to input said modified pseudo random patterns to said shift registers;

a mask to convert an indeterminate value in outputs from said shift registers into a state value of "0" or "1" to mask said indeterminate value; and

an output verifier to verify output results in which said indeterminate value is masked by said mask, said output results not containing said indeterminate value.

32-33. (CANCELLED)

34. (NEW) A testing apparatus for an integrated circuit comprising:

a plurality of shift registers, to which test patterns are inputted, configured with sequential circuit elements inside said integrated circuit;

a mask to specify a shift register in said plurality of shift registers which outputs an indeterminate value, based on external control signals, and to convert the indeterminate value, contained in the outputs from the specified shift register, into a state value of "0" or "1" to mask the indeterminate value; and

an output verifier to verify the masked output results of the specified shift register, from which output results the indeterminate value is excluded.

35. (NEW) The testing apparatus according to claim 34, wherein said output verifier includes a compressing means for compressing the masked outputs.

36. (NEW) An integrated circuit including sequential circuit elements, comprising:

a plurality of shift registers, to which test patterns are inputted, configured with said sequential circuit elements;

a mask to specify a shift register in said plurality of shift registers which outputs an indeterminate value, based on external control signals, and to convert the indeterminate value, contained in the outputs from the specified shift register, into a state value of "0" or "1" to mask the indeterminate value; and

an output verifier to verify the masked output results of the specified shift register, from which output results the indeterminate value is excluded.